



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	F	ILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/824,709	04/04/2001		Hideki Kabune	1-129 1768	
23400	7590	10/12/2005		EXAMINER	
POSZ LAW		•	YANCHUS III, PAUL B		
SUITE 101	12040 SOUTH LAKES DRIVE SUITE 101				PAPER NUMBER
RESTON, V	'A 2019	1	2116		

DATE MAILED: 10/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

1								
	Application No.	Applicant(s)						
Office Action Summer	09/824,709	KABUNE ET AL.						
Office Action Summary	Examiner	Art Unit						
<u> </u>	Paul B. Yanchus	2116						
The MAILING DATE of this communication appe Period for Reply	ears on the cover sheet with the co	orrespondence address						
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period with a failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	TE OF THIS COMMUNICATION 6(a). In no event, however, may a reply be tim ill apply and will expire SIX (6) MONTHS from to cause the application to become ABANDONED	l. ely filed he mailing date of this communication. D (35 U.S.C. § 133).						
Status								
1) Responsive to communication(s) filed on 19 Ju		•						
,—	action is non-final.	secution as to the merits is						
. —	3) Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.							
Disposition of Claims		· ·						
4)⊠ Claim(s) <u>1-3,6 and 7</u> is/are pending in the application.								
4a) Of the above claim(s) is/are withdrawn from consideration.								
5) Claim(s) is/are allowed.								
6)⊠ Claim(s) <u>1-3 and 6-7</u> is/are rejected.								
· <u></u>	7) Claim(s) is/are objected to.							
8) Claim(s) are subject to restriction and/or	election requirement.							
Application Papers								
9)☐ The specification is objected to by the Examiner	;							
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.								
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).								
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).								
11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.								
Priority under 35 U.S.C. § 119								
12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) ☐ All b) ☐ Some * c) ☐ None of:								
1. Certified copies of the priority documents have been received.								
2. Certified copies of the priority documents have been received in Application No								
3. Copies of the certified copies of the priority documents have been received in this National Stage								
application from the International Bureau (PCT Rule 17.2(a)).								
* See the attached detailed Office action for a list of the certified copies not received.								
,								
Attachment(s)								
1) Notice of References Cited (PTO-892)	4) Interview Summary							
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 	Paper No(s)/Mail Da 5) Notice of Informal Pa	te atent Application (PTO-152)						
Paper No(s)/Mail Date	6) Other:							

Application/Control Number: 09/824,709

Art Unit: 2116

DETAILED ACTION

In view of the arguments filed on 07/28/05, PROSECUTION IS HEREBY REOPENED.

New grounds of rejection set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

- (1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,
 - (2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of Curinger et al., US Patent no. 6,330,668 [Curinger].

Regarding claim 1, AAPA discloses an electronic control apparatus comprising:

Application/Control Number: 09/824,709

Art Unit: 2116

a plurality of power source circuits providing a plurality of power sources [dual power source circuit] of a plurality of different voltages [higher voltage and lower voltage, page 1, lines 20-23]; and

a microcomputer [one-chip microcomputer, page 2, line 1],

wherein any one of the plurality of power sources is used as a power source of the microcomputer [page1, lines 20-27].

AAPA does not explicitly disclose immediately resetting the microcomputer when a voltage abnormality is detected. Curinger discloses circuitry for monitoring the voltage supplied to a microcontroller circuit and resetting the microcontroller when the voltage is too high or too low [column 3, lines 21-26]. Curinger does not disclose any type of delay between the detecting of an abnormal voltage and the resetting of the microcontroller. Therefore it is interpreted that the microcontroller is reset immediately after the detection that the supplied voltage is too high or too low.

It would have been obvious to one of ordinary skill in the art to modify the AAPA apparatus to include the Curinger power monitoring and microcontroller resetting circuitry.

Resetting a microcomputer immediately after it is detected that a power source output is not in the proper voltage range ensures that the microcomputer will not perform incorrect calculations [column 1, lines 64-67 and column 2, lines 12-17].

Regarding claim 2, AAPA discloses that the dual power source circuit outputs a first voltage [higher voltage] that is applied to a peripheral circuit and an A/D converter and outputs a second voltage [lower voltage] that is lower than the first voltage to the oscillation circuit and the CPU [page 1, lines 20-27]. Curinger et al., as described above, discloses circuitry for detecting if

a voltage supplied to the microcomputer is too high or too low and resetting the microcomputer if one of the power sources is not set to a voltage in the respective specified ranges.

Regarding claim 6, AAPA discloses an electronic control apparatus comprising:

a plurality of power source circuits providing a plurality of power sources [dual power source circuit] of a plurality of different voltages [higher voltage and lower voltage, page 1, lines 20-23]; and

a microcomputer [one-chip microcomputer, page 2, line 1],

wherein any one of the plurality of power sources is used as a power source of the microcomputer [page1, lines 20-27].

AAPA does not explicitly disclose immediately resetting the microcomputer when a voltage abnormality is detected. Curinger discloses circuitry for monitoring the voltage supplied to a microcontroller circuit and resetting the microcontroller when the voltage is too high or too low [column 3, lines 21-26]. Curinger does not disclose any type of delay between the detecting of an abnormal voltage and the resetting of the microcontroller. Therefore it is interpreted that the microcontroller is reset immediately after the detection that the supplied voltage is too high or too low.

It would have been obvious to one of ordinary skill in the art to modify the AAPA apparatus to include the Curinger power monitoring and microcontroller resetting circuitry.

Resetting a microcomputer immediately after it is detected that a power source output is not in the proper voltage range ensures that the microcomputer will not perform incorrect calculations [column 1, lines 64-67 and column 2, lines 12-17].

Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Curinger et al., US Patent no. 6,330,668 [Curinger], in view of Carter, US Patent no. 6,298,449.

AAPA and Curinger, as described above, disclose detecting if any one of a plurality of power sources is not set to a voltage in respective specified ranges and immediately resetting a microcomputer if one of the power sources is not set to a voltage in the respective specified ranges. AAPA and Curinger do not explicitly disclose detecting if any of the plurality of power sources is not set to a current in respective specified ranges. Carter teaches detecting if current being input to a computer deviates from a predetermined range [column 5, lines 20-43, column 6, lines 8-23 and column 9, lines 14-16].

It would have been obvious to one of ordinary skill in the art to modify the AAPA and Curinger apparatus to include the Carter current detection circuitry. According to Carter, abnormal current levels can be a strong indication of a computer failure [column 5, lines 25-27]. Detecting abnormal current levels in addition to abnormal voltage levels in a computer system provides an extra level of fault detection to which leads to improved system reliability.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

Application/Control Number: 09/824,709 Page 6

Art Unit: 2116

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus October 6, 2005 LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100